

Excellence is not a Skill, its an Attitude

One Stop Shop for ARM & FPGA Security Technologies

Training Services (with practical hands-on labs):

ASIC/FPGA Verification

- -- Fundamentals & Advanced UVM
- -- SystemVerilog for Verification Engineers
- -- Code & Functionality Coverage Advanced Techniques

Arm Official

- -- Cortex-A/R/M for v6/7/8/9 Architectures
- -- All system IP (GIC, CMN, AMBA, CoreSight, etc.)
- -- TrustZone for Cortex-A & Cortex-M
- -- Optimization with SVE/SVE2/NEON
- -- Ethos-U for AI Acceleration

Security

- -- Side Channel Attack in Practice & Countermeasures
- -- Fault Injection in Practice & Countermeasures
- -- FPGA Security Bootcamp
- -- Embedded Systems Security Bootcamp
- -- Practical Threat Modeling

Altera FPGA

- -- Designing with Agilex Family
- -- SoC FPGA Design for HW & SW Engineers
- -- OpenVino and Al Suite
- -- Timing Closure with TimeQuest
- -- HDL for Low Power & Small Area
- -- Designing for High-Performance
- -- Clock Domain Crossing Techniques
- -- VHDL/Verilog Expert
- -- Altera FPGA Designer Program

Design Services

FPGA Design

- -- System Point of View
- (Hardware-Firmware-Software-Verification-Debug-Security)
- -- All FPGAs Vendors & Families
- (Altera, Xilinx, Microchip, Lattice)
- -- Software and BSP Development for
- SoC FPGAs & Soft Processors
- -- FPGA Security
- -- Timing Closure
- -- Al for FPGA
- -- High-Speed Interfaces & Protocols
- -- 5G Communication
- -- Verification with SV and UVM
- -- Advanced Optimization Techniques (Area, Speed, Power)
- -- Military

Embedded Software Design

- -- BSP Development for Arm based SoC
- -- Add Arm tool-flow to any vendor target device (ArmDS, Keil)
- -- Linux & RTOS
- -- Performance/Code Density Optimization

Security

- -- Threat Modeling & Risk Analysis
- -- Design Auditing
- -- Implementing Countermeasures
- -- Secure Boot
- -- Protecting Data-in-Transit and Data-at-Rest
- -- SCA and FI HW & SW Countermeasure
- -- Platform Attestation

For detailed training agenda and full syllabuses: www.HandsOn-Training.com

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